

## STRUCTURE OF THIN FILM TRANSISTOR AND MANUFACTURING METHOD THEREOF

### FIELD OF THE INVENTION

[0001] The present invention is related to a structure of a thin film transistor and a manufacturing method thereof, and more particularly to a structure of a thin film transistor applied to TFT-LCD and a manufacturing method thereof.

### BACKGROUND OF THE INVENTION

[0002] Thin film transistor liquid crystal Display (TFT-LCD) has become one of the most popular and modern information goods. As result of being light, small and portable, having a lower operating voltage, being free of harmful radiation and suited to production on large scale, TFT-LCD substitutes for cathode ray tube display as a caressed computer display device.

[0003] In accordance with the structure of TFT-LCD, Drain of TFT has a higher electric field while TFT is operating, and there should be an off-state leakage current resulted while the device is shut down, thereby the application of TFT-LCD being limited.

[0004] Presently, someone provides a lightly doped drain structure and a field induced drain structure for preventing TFT-LCD from the off-state leakage current. Fig. 1 illustrates a lightly doped drain structure of the prior art for solving the problem of the off-state leakage current. The structure includes an insulating substrate 11, a source/drain layer 12, a gate insulating layer 13 and a gate layer 14, wherein the source/drain layer 12 further includes a drain 121, a lightly doped drain 1211, a channel 122, a source 123 and a lightly doped source

1231. The electric field of the drain 121 is reduced by means of adding lightly doped regions (i.e. the lightly doped drain 1211 and the lightly doped source 1231) corresponding to the original source 123 and the original drain 121 respectively near the channel 122, so as to prevent from the leakage current. However the TFT-LCD with the lightly doped regions is complex and hard to manufacture. Furthermore the resistance will increase because of the lightly doped degree. As result of the series resistance of the drain 121 and the source 123 increasing, the operating speed of the device reduces and the power dissipation increases.

[0005] Moreover, another improving structure of field-induction drain has been disclosed. However it has to add an extra photolithographic process for manufacturing the improving structure. The more photolithographic processes are introduced, the more mis-alignment and infected defects are resulted. Therefore, the cost and the manufacturing time of the improving structure must increase and the yield reduces.

[0006] Hence, the present invention is attempted to improve the prior art and provides a structure of a thin film transistor applied to a TFT-LCD and a manufacturing method thereof for preventing TFT-LCD from the leakage current.

#### SUMMARY OF THE INVENTION

[0007] It is one object of the present invention to provide a structure of a thin film transistor applied to TFT-LCD and a manufacturing method thereof.

[0008] It is another object of the present invention to provide a structure of a thin film transistor and a manufacturing method thereof for preventing TFT-LCD from the leakage current.

[0009] According to the present invention, the method for manufacturing a thin film transistor, includes steps of providing an insulating substrate, sequentially forming a source/drain layer, a primary gate insulating layer, and a first conducting layer on the insulating substrate, etching the first conducting layer to form a primary gate, sequentially forming a secondary gate insulating layer and a second conducting layer on the primary gate, and etching the second conducting layer to form a first secondary gate and a second secondary gate.

[00010] Certainly, the insulating substrate can be a glass.

[00011] Certainly, the source/drain layer can be a high-doping semiconductor layer.

[00012] Certainly, the high-doping semiconductor layer can be high-doping polycrystalline silicon.

[00013] Preferably, the source/drain layer includes a drain, a channel and a source.

[00014] Preferably, the channel has a length equal to a sum of a length of the primary gate, a width of the secondary insulating layer, a length of the first secondary gate and a length of the second secondary gate.

[00015] Certainly, the primary gate insulating layer can be one selected from a silicon nitride ( $\text{SiN}_x$ ), a silicon oxide ( $\text{SiN}_x$ ), a silicon oxide nitride ( $\text{SiO}_x\text{N}_y$ ), a tantalum oxide ( $\text{TaO}_x$ ), an aluminum oxide ( $\text{AlO}_x$ ) and a mixture thereof.

[00016] Certainly, the first conducting layer can be one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof.

[00017] Certainly, the step (c) can be executed by means of a reactive ion etching.

[00018] Certainly, the secondary gate insulating layer can be one selected from a silicon nitride ( $\text{SiN}_x$ ), a silicon oxide ( $\text{SiN}_x$ ), a silicon oxide nitride ( $\text{SiO}_x\text{N}_y$ ), a tantalum oxide ( $\text{TaO}_x$ ), an aluminum oxide ( $\text{AlO}_x$ ) and a mixture thereof.

[00019] Certainly, the second conducting layer can be one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof.

[00020] Certainly, the step (e) can be executed by means of a reactive ion etching.

[00021] According to the present invention, the structure of a thin film transistor includes an insulating substrate, a source/drain layer disposed on the insulating substrate, a primary insulating layer disposed on the source/drain layer, a primary gate disposed on the primary insulating layer, a secondary insulating layer disposed on the primary insulating layer, and a secondary gate disposed on the secondary insulating layer and insulated from the primary gate via the secondary insulating layer.

[00022] Preferably, the secondary insulating layer further includes a first secondary insulating layer and a second secondary insulating layer.

[00023] Preferably, the secondary gate further includes a first secondary gate and a second secondary gate disposed on the first secondary insulating layer and the second secondary insulating layer respectively.

[00024] Certainly, the insulating substrate can be a glass.

[00025] Certainly, the source/drain layer can be a high-doping semiconductor layer.

[00026] Certainly, the high-doping semiconductor layer can be high-doping polycrystalline silicon.

[00027] Preferably, the source/drain layer includes a drain, a channel and a source.

[00028] Preferably, the channel has a length equal to a sum of a length of the primary gate, a width of the secondary insulating layer, and a length of the secondary gate.

[00029] Certainly, the primary gate insulating layer can be one selected from a silicon nitride ( $\text{SiN}_x$ ), a silicon oxide ( $\text{SiN}_x$ ), a silicon oxide nitride ( $\text{SiO}_x\text{N}_y$ ), a tantalum oxide ( $\text{TaO}_x$ ), an aluminum oxide ( $\text{AlO}_x$ ) and a mixture thereof.

[00030] Certainly, the first conducting layer can be one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof.

[00031] Certainly, the primary gate can be formed by means of a reactive ion etching.

[00032] Certainly, the secondary gate insulating layer can be one selected from a silicon nitride ( $\text{SiN}_x$ ), a silicon oxide ( $\text{SiN}_x$ ), a silicon oxide nitride ( $\text{SiO}_x\text{N}_y$ ), a tantalum oxide ( $\text{TaO}_x$ ), an aluminum oxide ( $\text{AlO}_x$ ) and a mixture thereof.

[00033] Certainly, the second conducting layer can be one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum

(TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof.

[00034] Certainly, the secondary gate can be formed by means of a reactive ion etching.

[00035] According to the present invention, the structure of a thin film transistor includes an insulating substrate, a source/drain layer disposed on the insulating substrate, a primary insulating layer disposed on the source/drain layer, a primary gate disposed on the primary insulating layer, at least a secondary insulating layer disposed on the primary insulating layer, and at least a secondary gate disposed on the at least a secondary insulating layer and insulated from the primary gate via the at least a secondary insulating layer.

[00036] Certainly, the insulating substrate can be a glass.

[00037] Certainly, the source/drain layer can be a high-doping semiconductor layer.

[00038] Certainly, the high-doping semiconductor layer can be high-doping polycrystalline silicon.

[00039] Preferably, the source/drain layer includes a drain, a channel and a source.

[00040] Preferably, the channel has a length equal to a sum of a length of the primary gate, a width of the at least secondary insulating layer, and a length of the at least a secondary gate.

[00041] Certainly, the primary gate insulating layer can be one selected from a silicon nitride ( $\text{SiN}_x$ ), a silicon oxide ( $\text{SiN}_x$ ), a silicon oxide nitride ( $\text{SiO}_x\text{N}_y$ ), a tantalum oxide ( $\text{TaO}_x$ ), an aluminum oxide ( $\text{AlO}_x$ ) and a mixture thereof.

[00042] Certainly, the at least a secondary gate insulating layer can be one selected from a silicon nitride ( $\text{SiN}_x$ ), a silicon oxide ( $\text{SiO}_x$ ), a silicon oxide nitride ( $\text{SiO}_x\text{N}_y$ ), a tantalum oxide ( $\text{TaO}_x$ ), an aluminum oxide ( $\text{AlO}_x$ ) and a mixture thereof.

[00043] Now the foregoing and other features and advantages of the present invention will be more clearly understood through the following descriptions with reference to the drawings, wherein:

#### BRIEF DESCRIPTION OF THE DRAWINGS

[00044] Fig. 1 illustrates a lightly doped drain structure of the prior art for solving the problem of the off-state leakage current;

[00045] Figs. 2 (a) – 2 (e) illustrate the steps of manufacturing the thin film transistor according to the preferred embodiment of the present invention;

[00046] Fig. 3 illustrates electricity properties of the present invention compared with those of the prior art.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[00047] Figs. 2 (a) – 2 (d) illustrate the steps of manufacturing the thin film transistor according to the preferred embodiment of the present invention. The method for manufacturing a thin film transistor includes several steps. First, an insulating substrate 21 is provided and a source/drain layer 22, a primary gate insulating layer 23, and a first conducting layer 241 are sequentially formed on the insulating substrate 21, shown in Fig. 2 (a). Secondly, the first conducting layer 241 is etched to form a primary gate 24, shown in Fig. 2 (b). Thirdly, a secondary gate insulating layer 25 and a second conducting layer 26 are sequentially formed on the primary gate 24, shown in Fig. 2 (c). Finally, the

second conducting layer 26 and the secondary gate insulating layer 25 are etched to respectively form a first secondary gate 271 and a second secondary gate 272, and a first secondary gate insulating layer 251 and a second secondary gate insulating layer 252, shown in Fig. 2 (d). As to Fig. 2 (e), it illustrates the bias status of the thin film transistor including a source bias voltage (VS) 28, a gate/source bias voltage (VGS) 29 and a drain/source bias voltage (VDS) 210.

[00048] According to the above embodiment of the present invention, the insulating substrate 21 is a glass substrate, the source/drain layer 22 is a high-doping semiconductor layer, and the high-doping semiconductor layer is high-doping polycrystalline silicon. Furthermore, the source/drain layer 22 includes a drain 221, a channel 222 and a source 223. Meanwhile, the channel 222 has a length equal to a sum of a length of the primary gate 24, a width of the first secondary insulating layer 251 and the second secondary insulating layer 252, a length of the first secondary gate 271 and the second secondary gate 272.

[00049] As to the primary gate insulating layer 23 and the secondary gate insulating layer 25, they can be one selected from a silicon nitride ( $\text{SiN}_x$ ), a silicon oxide ( $\text{SiO}_2$ ), a silicon oxide nitride ( $\text{SiO}_x\text{N}_y$ ), a tantalum oxide ( $\text{TaO}_x$ ), an aluminum oxide ( $\text{AlO}_x$ ) and a mixture thereof. However the first conducting layer 241 and the second conducting layer 26 are one selected from chromium (Cr), molybdenum (Mo), tantalum (Ta), tantalum molybdenum (TaMo), tungsten molybdenum (WMo), aluminum (Al), aluminum silicon (AlSi), copper (Cu) and a mixture thereof. Meanwhile, the first conducting layer 241, the second conducting layer 26 and the secondary gate insulating layer 25 are etched by means of a reactive ion etching.

[00050] Referring to Fig. 3, it illustrates electricity properties of the present invention compared with those of the prior art. As result of operating the thin



film transistor according to the bias status of Fig. 2 (e), the thin film transistor of the present invention causes a lower leakage current. In Fig. 3, when the thin film transistor of the present invention and the thin film transistor of the prior art are operated in the same condition ( $V_{DS}=10V$ ), the leakage current caused by the present invention is lower than that caused by the prior art. While  $V_{DS}=15V$ , the leakage current ( $1 \times 10^{-9}A$ ) of the present invention is 100 times as that ( $1 \times 10^{-7}A$ ) of the prior art.

[00051] Accordingly, the present invention reduces the electric field of the drain region by means of providing a thicker gate insulating layer, so as to improve the problem of the high off-state leakage current of a thin film transistor. Comparing with the prior art, the present invention introduces four photolithographic processes equal to the traditional one, but doesn't have to add an extra photolithographic process. Therefore, the present invention can solve the drawbacks of the prior art and be practicability.

[00052] Although the present invention has been described and illustrated in detail, it is to be clearly understood that the same is by the way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.